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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,901	02/10/2004	Fook-Luen Heng	END920030090US1 (16992)	3048

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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,901	HENG ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 02/10/2004. **Claims 1-15** are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-15** are rejected under 35 U.S.C. 102(e) as being anticipated by **Granik et al. (US Patent No. 6,928,634).**

Referring to claim 1 and similarly recited claims 6 and 11, Granik et al. disclose a method (claim 1), a system (claim 6), and a method executed by a computer (claim 11), respectively, for lithographic process window optimization of an integrated circuit layout on a wafer and of superimposable masks and mask levels for fabrication of the integrated circuit layouts that are illuminated by beams of light radiation from a range of directions, said method comprising:

specifying a preliminary set of printed circuit feature edge locations (abstract, Fig. 1A; col. 1, ll. 38 to col. 2, ll. 7; Fig. 5, step 122, col. 5, ll. 46-60);

specifying a set of linked constraints on allowable positions for the edges of said circuit features (abstract; col. 1, ll. 38 to col. 2, ll. 7; Figs. 3A-3B; col. 3, ll. 56 to col. 5, ll. 12);

initially centering trust regions at the preliminary locations of said circuit feature edges (Fig. 3A, col. 3, ll. 56 to col. 4, ll. 54; col. 5, ll. 32-44);

computing models of the intensity of images projected within said trust region (Fig. 1A, col. 1, ll. 49 to col. 2, ll. 38; Fig. 3A, col. 3, ll. 56 to col. 4, ll. 54); and

adjusting shapes provided on said masks and intensities of said light beams illuminating the masks to project images on the wafer which satisfy the linked set of constraints over as wide a range of exposures as possible based on the computing models (Fig. 3A, col. 3, ll. 56 to col. 4, ll. 54).

Referring to claim 2 and similarly recited claims 7 and 12, Granik et al. disclose a method/ a system/ a method executed by a computer as claimed in claims 1, 6, and 11, respectively, wherein the model region at each edge location is recentered upon the printed edge of said circuit layout reaching the exterior of said model region (col. 1, ll. 39-48; Fig. 3A, col. 3, ll. 56 to col. 4, ll. 54).

Referring to claim 3 and similarly recited claims 8 and 13, Granik et al. disclose a method/ a system/ a method executed by a computer as claimed in claims 1, 6, and 11, respectively, wherein said integrated circuit features are simultaneously optimized on a plurality of mask levels through the linked involvement of a plurality of circuit feature edges (abstract; col. 2, ll. 51-61; Figs. 4-6A and 6B; col. 5, ll. 13 to col. 8, ll. 8).

Referring to claim 4 and similarly recited claims 9 and 14, Granik et al. disclose a method/a system/ a method executed by a computer as claimed in claims 1, 6, and 13, respectively, wherein said allowable positions of said edges are shiftable

within a range in which the variation of image intensity at the image sidewalls is approximately linear ("image slope") or quadratic in nature (Fig. 1B; col. 1, ll. 56 to col. 2, ll. 7).

Referring to claim 5 and similarly recited claims 10 and 15, Granik et al. disclose a method/ a system/ a method executed by a computer as claimed in claims 4, 9, and 14, respectively, wherein said allowable shifts in the edges are implemented in parallel with trust region constraints on edge positions to effect said circuit layout optimization (abstract; col. 2, ll. 51-61; Figs. 4-6A and 6B; col. 5 ll. 13 to col. col. 8, ll. 8).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuyen To
Patent Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER